

AMENDMENTS TO THE CLAIMS

1-19. (Canceled)

20. (Currently Amended) A method of forming an integrated circuit comprising:

forming a performance circuit occupying a first well of an integrated circuit substrate;

forming a protection circuit occupying a second well of the integrated circuit substrate separate from the first well, wherein forming the protection circuit includes:

forming a plurality of unit cells, the plurality of unit cells separated from each other to form a plurality of islands in the second well surrounded by the second well, each of the plurality of unit cells comprised of:

a block of a first doped region of a first dopant in the second well of the integrated circuit substrate occupying an area of the substrate sufficient to support a contact to the doped region, the first doped region forming an anode of a diode,

a junction region ~~of the integrated circuit substrate~~ completely surrounding the first doped region ~~and separating the first doped region from the second well,~~ and

a contact to the doped region, wherein  
the second well is doped with a first concentration of a second dopant,

forming a third doped region in the second well adjacent the junction region, the third doped region surrounding the plurality of cells and doped with a greater concentration of the second dopant, the third doped region forming a cathode of the diode; and

coupling the protection circuit to the performance circuit.

21. (Previously Presented) The method of claim 20, wherein forming a performance circuit includes forming a CMOS configuration.

22. (Previously Presented) The method of claim 21, wherein coupling the protection circuit to the performance circuit includes coupling the protection circuit to a p-channel device of the CMOS configuration.

23. (Previously Presented) The method of claim 21, wherein forming a protection circuit includes forming the diode and coupling the protection circuit to the performance circuit includes coupling the diode to a p-channel device of the CMOS configuration.

24-26. (Canceled.)

27. (Previously Presented) A method of forming an integrated circuit comprising:

forming a first protection circuit on the integrated circuit substrate;

forming a performance circuit occupying a first well of an integrated circuit substrate, wherein forming a performance circuit includes:

forming a unit transistor device having a drain region comprised of a first doped region of the integrated circuit substrate occupying an area sufficient to support a contact to the first doped region;

forming a gate region of the integrated circuit substrate surrounding the first doped region; and

forming a contact to the first doped region;

forming a second protection circuit occupying a second well of the integrated circuit substrate separate from the first well, the second protection circuit including a plurality of unit cells forming a plurality of islands in the second well surrounded by a second doped region; and

coupling the second protection circuit between the first protection circuit and the contact.

28. (Previously Presented) The method of claim 27, wherein the first doped region is doped with of a first dopant in the first well of the substrate, the first well being doped with a concentration of a second dopant and wherein forming a performance circuit further comprises:

forming a source region of the transistor doped with the first dopant in the first well separated from the drain region by the gate to form a unit transistor.

29. (Previously Presented) The method of claim 28, wherein forming a performance circuit includes:

forming a plurality of unit transistors.

30. (Currently Amended) A method of forming an integrated circuit comprising:

forming a performance circuit occupying a first well of an integrated circuit substrate;

forming a protection circuit occupying a second well of the integrated circuit substrate separate from the first well, wherein forming the protection circuit includes:

forming a plurality of unit cells, the plurality of unit cells separated from each other to form a plurality of islands in the second well surrounded by the second well, each of the plurality of unit cells comprised of:

a block of a first doped region of a first dopant in the second well of the integrated circuit substrate occupying an area of the substrate sufficient to support a contact to the doped region,

a junction region of the integrated circuit substrate completely surrounding the first doped region and ~~separating the first doped region from the second well~~, and

a contact to the doped region, wherein the second well is doped with a first concentration of a second dopant,

forming a third doped region in the second well adjacent the junction region, the third doped region surrounding the plurality of cells and doped with a greater concentration of the second dopant; and

coupling the protection circuit to the performance circuit.

31. (Previously Presented) The method of claim 30, wherein forming a performance circuit includes forming a CMOS configuration.

32. (Previously Presented) The method of claim 31, wherein coupling the protection circuit to the performance circuit includes coupling the protection circuit to a p-channel device of the CMOS configuration.

33. (Previously Presented) The method of claim 31, wherein forming a protection circuit includes forming the diode and coupling the protection circuit to the performance circuit includes coupling the diode to a p-channel device of the CMOS configuration.

34. (Canceled)

35. (Previously Presented) The method of claim 30, wherein the first concentration of a second dopant forms an N-type material in the second well.

36. (Previously Presented) The method of claim 30, wherein the second concentration of the second dopant forms an N<sup>+</sup> material in the third doped region.